AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor package comprising:

at least one plate-like mount;

a semiconductor chip having at least one electrode formed on a top surface thereof, and mounted on said plate-like mount such that a bottom surface of said semiconductor chip is in contact with said plate-like mount;

at least one lead element having an outer portion ~~arranged to be flush~~ that is substantially coplanar with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said lead element is spaced apart from the top surface of said semiconductor chip without being mechanically connected to said chip;

a bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element; and

an enveloper sealing and encapsulating said plate-like mount, said semiconductor chip, the inner portion of said lead element, and said bonding-wire element.

2. (previously presented) A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is directly and electrically connected to the second electrode of said semiconductor chip, using an electrically conductive paste.

3. (original) A semiconductor package as set forth in claim 2, wherein said semiconductor chip is constructed as a MOSFET chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

4. (original) A semiconductor package as set forth in claim 3, wherein said MOSFET chip is formed as a high power type, and the source electrode has a larger area than that of said gate electrode.

5. (original) A semiconductor package as set forth in claim 4, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

6. (original) A semiconductor package as set forth in claim 1, wherein said electrode is defined as a first electrode, and said lead element is defined as a first lead element,

said semiconductor chip further having a second electrode formed on the top surface thereof,

said semiconductor package further comprising: a second lead element having an outer portion arranged to be flush with said plate-like mount, and an inner portion deformed and shaped to overhang said semiconductor chip such that an inner end of said second lead element is spaced apart from the top surface of said semiconductor chip; and at least one bonding-wire element bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said second lead element.

7. (original) A semiconductor package as set forth in claim 6, wherein said semiconductor chip is constructed as a MOSFET chip having a drain electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, with said respective first and second electrodes being defined as a source electrode and a gate electrode, and said plate-like mount has at least one lead element extending therefrom.

8. (original) A semiconductor package as set forth in claim 7, wherein said MOSFET chip is formed as a high power type, and the source electrode has a larger area than that of said gate electrode.

9. (original) A semiconductor package as set forth in claim 8, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

10. (original) A semiconductor package as set forth in claim 1, wherein said semiconductor chip has another electrode formed on a bottom surface thereof and electrically connected to said plate-like mount, and said plate-like mount has at least one lead element extending therefrom.

11. (original) A semiconductor package as set forth in claim 10, said semiconductor chip is constructed as a diode chip, with one of the electrodes formed on the top and bottom surfaces of said semiconductor chip being defined as an anode electrode, the remaining electrode being defined as a cathode electrode.

12. (original) A semiconductor package as set forth in claim 11, wherein said diode chip is formed as a high power type.

13. (original) A semiconductor package as set forth in claim 12, wherein the sealing and capsulation of said plate-like mount in said enveloper is carried out such that a bottom surface of said plate-like mount is exposed to outside.

14-22. (cancelled)

23. (currently amended) A semiconductor package comprising:

a planar mounting element;

a semiconductor chip having at least one electrode formed on a top surface thereof, said semiconductor chip being mounted on said planar mounting element such that a bottom surface of said semiconductor chip is in contact with said planar mounting element;

a first lead element having an outer portion ~~arranged to be flush~~ that is substantially coplanar with said planar mounting element, and an inner portion deformed and shaped to overlap said semiconductor chip such that an inner end of said lead element is spaced apart from and directly overlies the top surface of said semiconductor chip without being mechanically connected to said chip;

a bonding-wire bonded at ends thereof to the electrode of said semiconductor chip and the inner end of said lead element; and

an enveloper sealing and encapsulating said planar mounting element, said semiconductor chip, the inner portion of said lead element, and said bonding-wire.

24. (cancelled)

25. (new) A semiconductor package comprising:

an island;

a MOSFET chip mounted on said island and having a

source electrode and a gate electrode formed on a top surface thereof;

a first lead element having an inner portion extending from said island;

a second lead element having an inner portion directly connected to the source electrode of said MOSFET chip;

a third lead element having an inner portion which is spaced apart from the top surface of said MOSFET chip;

a bonding-wire element bonded at respective ends thereof to the gate electrode of said MOSFET chip and the inner portion of said third lead element; and

an enveloper sealing and encapsulating said island, said MOSFET chip, the inner portions of said first, second and third lead elements, and said bonding-wire element.

26. (new) The semiconductor package as set forth in claim 25, wherein outer portions of said first, second and third lead elements project outward from said enveloper and are substantially coplanar with each other.

27. (new) The semiconductor package as set forth in claim 25, wherein said island is connected to a drain electrode formed on a bottom surface of said MOSFET chip.

28. (new) The semiconductor package as set forth in claim 25, wherein said enveloper is formed as a molded resin enveloper.

29. (new) The semiconductor package as set forth in claim 25, wherein said first lead element is derived from a first lead frame, and said second and third lead elements are derived from a second lead frame.